ABSTRACT OF THE DISCLOSURE

A processor has an instruction set A and an instruction set B. A system instruction decoder decodes a system instruction that specifies the operating mode of the processor, the system instruction not being included in either the instruction set A or the instruction set B. A system instruction execution controller receives a decoded signal from the system instruction decoder, which has decoded an instruction requiring changeover of the instruction set, and sets the value of a instruction mode register. On the basis of the value in the instruction mode register, an instruction set changeover unit selects the instruction set to be used.